## Information for the 1000 Series Dart Game

The following pages are being made available to those that need technical information on our older dart games. We realize that it is not in any way complete, and that some of the information is hand drawn, but we are furnishing what we have in case it will help someone. There are no parts available for these older games, nor is anyone at Arachnid familiar with them. We hope that what we can provide will be of some assistance.

This classification consists of 5 sections $A D-100 \mathrm{X}-\mathrm{X}-\mathrm{X}-\mathrm{X}$
(1) AD- for Arachnid Darts
(2) 4 numbers - the appearance of the game etc.
$1000=$ flat top to lower cabinet mat type score inhibit.
1001 = sloping top to lower cabinet 'Player Change' score inhibit.
1002 = wall mounting vending game
$1003=$
1100 = homegame board - numbers embossed on spider
(3) 1 letter - the type of game available

A $=301$ Game
B $\quad=$ Round the Clock
C = Count up from Zero
D $\quad=301$ Game ending on a Double Score
$\mathrm{E} \quad=301$ Game starting and ending on a Double
$\mathrm{F}=$ Cutthroat
G $\quad=$ Games $A, D$, and $E$ - pre-set with links
$\mathrm{H}=$ Games $A, B, C, D, E$, and $F$
(4) 1 number - the type of dartboard
$1=$ diaphragm \& switches type
2 = diaphragm \& switches type with 'free' segments
$=$ conductive rubber type 301 game only
2 = conductive rubber type all games iu double bullseye
5 = permanently fixed segments, no switches, etc.
(5) 1 letter - the electronics package

$$
\begin{aligned}
& \mathrm{A} \\
& \mathrm{~B} \\
& \mathrm{C} \\
& \mathrm{C} \\
& =8 \text { P.C. Cards on motherboard } \\
& =1 \text { logic card on shorter motherboard } \\
& \text { lith microcomputer }
\end{aligned}
$$

As an example:

| Vending Machines | $\mathbf{1}-\mathbf{2 5}$ | are type | $A D-1000-A-1-A$ |
| :--- | ---: | :--- | :--- | :--- |
|  | $\mathbf{2 6} \mathbf{- 5 0}$ are type | $A D-1001-A-1-A$ |  |
|  | $\mathbf{5 1} \mathbf{- 2 0 0}$ | are ty e | $A D-1001-A-2-B$ |

The low cost homegame is type AD-110 -H-5.

$$
\begin{aligned}
& \text { COPY NO. } 161 \\
& \text { I iSSUE; aQ } \\
& \text { CONTENTS } \\
& \text { SECTI ON 1. rOutIne Electrical Specification } \\
& \text { 2. Mach ne Operation } \\
& \text { 3. Cali net and fixtures } \\
& \text { 4. Dart board } \\
& \text { El oct toni cs Package } \\
& 6 \text { Fault di agnoses--preliminary listing } \\
& \text { 7. Mai nt nance }
\end{aligned}
$$

CAUII ON This inf or nation must be treated as preliminary and nay be subject to revision by subsequent documents.

## SECTI ON 2 <br> MACHI NE OPERATI ON

2. 1 THE 'Gane of Darts: the 301 gane rules
'The players start with a score of 301 and each dart's score' subtracted from it. The players total therefore decreases and approaches zero as the gane progresses. Pl ayer takes turn at throwing three darts. As each dart scores, its score is subtracted from that players total and his new total is displayed
dhenéAfter a pl ayer has thrown all his three darts the player and the next person takes his turn.

To WIN a gane, a player has to make a score which reduces hi s score to zero exactly. This may happen 'with the first, second or third dart of his turn. When a player's score equal s exactly ZERO the machine will:
(i) set up a GAME OVER situation
(ii) indicate that payer has VON
(iii) prevent any inputs from having any effect,
except for coin insertion
(iv) drive a gong

As a pl ayers score approaches ZERO, he may hit a number which is greater than he requires to WIN. As with a WIN, this could happen on the first, second or third dart. This situation is called a BUST. When a BUST situation occurs then the. nachi ne will:
(i) recall the player's score immediately prior to his present
turn and display it. If a player BUSTS on his first dart, he
will not notice any change in his score but busting on darts
2 or 3 he will notice that his score reverts to what it was bef ore throwing the first dart.
(ii) turn on the "BUST" I amp
(iii)drive a buzzer
(iv) prevent any further score from being recorded.

After achi eving a bust the player then abandons his turn, presses the plaver change button and recovers his darts from the board. W i th this action the next player is brought into the gane and the BUST Iamp is cleared. (The score for the player who bust is not changed by pressing the player change button).

The Displays on the English Mark Darts machl ne.

2. 3 Other Outputs. Alonze

The Bust buzzer and the $\mathbf{W}$ n gong are both inside the upper cabi nets and the Board IIIIunination lamp has a socket on the right hand side of the upper cabi net.

The Board IIIumi nation I amp is turned. on after the first coin is inserted and goes off about 1 second after the gane has been won.
2. 4 The Action of the Coin Mechani sm

The first coin inserted after either
a) the nachi ne has been switched on, or
b) the machine is in a WN (or GAMEOVER) condition, or (cl the 'player change' button has been pressed, will set up the gane for 1 pl ayer

Subsequent coins will add to the number of players in the gane.

## NUMBERI NG SYSTEM

A I si gnal s going into or coming out of the indi vi dual circuit cards have been designated a uni que number.

- The simple code has either $a \quad P$ or an $L$ initially and this signifies whether the ACTIVE portion of that signal is long term or transitory.
- The second digit is either a 0 or a 1. Again this designates the ACTI VE part of the pulse or level to be a logic 0 or a logic 1.
-From then on they are listed numerically.


## CARDS AND PI N NUMBERS

Under neath each card type is a bracket number. That is the pin number associated with that signal. On occasions where there are 4 similar signals, going to, or coming from the 4 PSD cards the signals are subscripted $a, b, c, d$. In these cases 4 pin numbers appear in the listing an these are in the sequence of $a, b, c, d$.

The nachi ne. comprises an upper and I ower cabi net. The I ower cabi net houses sol ely the coin mechani sm and is accessible onl y from the front in the coin door. Al the renai nder of the game is contai ned within the upper cabinet. Access to this is through the door on the rear.

The wiring di agram drawing SADO1 6, provi des a schenatic representation of the wiring within the cabi net and al so gives the col ours of the indi vidual wires in the cableform

The Component Parts List details all the major itens in the cabinets and from these tho data sheets, the essential features of this machi ne can be recognized.

Buzzer and Gong
The two devi ces are activated during the course of a game, the buzzer to tell the pl ayer that he has gone beyond zero and the gong to tell him that he has achi eved zero.

The buzzer is driven from a 115V A. C. si gnal and may need occasional adjustment of the screw hol ding its mounting bracket to the cabi net (the lower of the two screws) to obtain the loudest buzz.

The gong is driven from a $24 V$ A. $C$. signal and has no' means of adj ust nent .

## 3. 3 Coi n Mechani sm

The need for regual $r$ cleaning of this item is the same as for coin mechani sns generally in vending machi nes. (Notes on this are to be found in section 7). The optional resistor Rl of 100 ohm shown on the cabi net wiring schedule (Drwing number SAD0126) prevents the [ machine from giving free games when the coin door is hit violently, causing the microswitch to make a momentorary contact.


Each segment's suitch contacts are connected to a printed circuit card which is assenbled to encircle the outer ring of switches. (The card is 2/2' wi de by 48" long when laid flat prior to assenbly).

The si ngles, doubl es and triples are connected by red, bl ue and white wires respectively. A common line joins all other contacts of the 81 switches.

This printed circuit card contains an encoding diode natrix whi ch encodes each score into a plain bi nary word of 1, 2, 4, 8, 16 and 32. Drawing number SAD0121 illustrates this technique.

A cabl ef orm connects this matrix to PL9 of the Mbtherboard.


## 5. 1 Component Parts

The electronics package comprises 8 plug in printed circuit component cards (daughter cards) approxi natel y 8" x 5". Which fit into a printed circuit notherboard. The notherboard is approxi nately 21" $x$ 8" and houses the 4 sets of the 7 segment displ ays, the lamps which illuminate the various captions and edge connector to connect to the cabi net cable.forns.

Of the 8 plug in cards, 4 are identical. Giving 5 different card types. Each type is described in the sections following the notherboard description.

Each of the card types has a keying sl ot in the connect or edge to prevent incorrect insertion of either the wrong card type or that pl ug or the right card type but inverted.
5. 2 The Mbther board

The Motherboard is a printed circuit card containing all the interconnecting links of the 8 daughter boards and the links to the LED displays. It al so serves as a fixing point for the reservoir capacitor for the maj or +5 volt logic supply line.

Tuo edge connectors, $P L 9$ and $P L 10$, connect it to the cabi net cabl ef orm and $8 \frac{1}{2}$ " screvs fix the notherboard to the front of the upper cabi net.

The description of the operation of the el ectronics package is cont ai ned in mai nly the indi vidual sections for each card type but here signal s appear on the motherboard, then these signals are assigned a code and are described fully in the subsequent signal description lists. This has been made part of the section on the notherboard for convienience.

| $\begin{aligned} & \text { SI GNAL } \\ & \text { CODE } \end{aligned}$ | SOURCE AND DESTI NATI CIN | CHARACTERI STI CS AND FUNCTI ON (TTL LEVELS WFERE NOT OTHERWSE STATED) |
| :---: | :---: | :---: |
| PO- 01 | Matrix to SPC <br> ( 13 | Decoded bi nary 1 of score. Noisy due to severe' conta bounce. 50 msec to be |
| PO- 02 | (11 | 2 allowed for bounce. |
| PO- 03 | ( | $4 \quad(1=+5 v \quad 0=+0.7 v)$ |
| PO- 04 |  | 8 " |
| PO- 05 | (21 | 16 |
| PO-06 | ( 213 | 32 |
| PO- 07 | SPC to GPM <br> (I) <br> (44) | 15 msec when ANY score is nade. Sets IC19 on GPM to control loading ' number of players playing' register ( I C18) . |
| PI-08 | $\begin{array}{lll} S P C & \text { to } & \text { TSO } \\ (15) & & (\mathbf{2 )} \end{array}$ | Pulse train, number of 'pulses equals score. Used to Ioad 3 decade counter ( $3 \times$ 74192's) on TSD. Approx 10 KHz . <br> -- Only used in AD1000 Mbdels with Temporary Score Dis |
| PI-09 | SPC to GPM <br> $(17)$ $(53)$  | as P1-08. Utinate destination is one of 4 PSD's controlled by 'Players turn' register (IC11 on GPM.! |
| $\mathbf{P q}-10^{\prime}$ | Coin Mechanis $\pm 0 \operatorname{GPM}(4,1)$ | ) A closing contact to 0 volts for a coin inserted into into mechani sm Significant bounce/ noise to be expected. <br> ( Exact anount dependent on mechanism). |
| PO-11 | Player change switch to GPF <br> (20) | A push button contact to 0 volts to sequence 'player turn' register round by 1 (ICll on GPM. Bounce dependent on contact type. |
| PO-12 | GPM to VBD <br> (34)  $(12)$ | 15 nsec. Derived from 'coin inserted'. Resets WIN register, IC13, on VBD. |
| PO-13 | GPM to VBD <br> (33)  (33) | 15 nsec. Derived from'switch on reset' circuit. Se WIN register. |
| P1-14 |  | number not allocat ed. |
| PO-15 | $\left\{\begin{array}{c} \mathbf{G P M} \mathbf{t o} \text { PSD } \\ (9,12,11,(55) \\ 10) \end{array}\right.$ | 15 nsec. Derived from both 'coin inserted' or 'switc on reset'. Clocks 3 decade counters ( $3 \times$ 74192's) on PSD for a parallel load. If L1-31 is a 1 then 301 is I oad into counters (see PO-20 for other condition). |
| PI-16 | GPM to TSD <br> (28)  (I) | 15 nsec. Derived from both 'coin inserted' or 'playe change'. Resets 3 decade counters on TSD to zero. -- Only used in AD1000 Mbdels with Temporary Score Dis |
| PO-17 | $\begin{array}{lll} \text { GPM } & \text { to } & \text { WBD } \\ (13) & & (35) \end{array}$ | 15 nsec. Effectively PI-16. Resets BUST register (I on UBD and produces reset or transfer pulses onwards PSD (see PO-19 and PO 20). |
| P1-18 | $\left(\begin{array}{ll} \text { GPM to } & \text { PSD } \\ (18,21 & \text { (2) } \\ 22,23) & \end{array}\right.$ | Pulse train. Derived from SPC, gated on GPM Used t count up the 3 decade counters on the selected PSD. |
| PO-19 | $\left\{\begin{array}{l} \text { WBD to PSD } \\ (10,9,7,8) \end{array}\right.$ | 15 nsec. Deri ved from PO 12 and ' Reset Bust Regi ster (PO-17. Transfers new valid score into display regis $\left(\begin{array}{lll}3 & x & 7475 \\ \text { s }\end{array}\right)$ on PSD. |

SI GNAL DESCRI PTI ON LI ST

| $\begin{gathered} \text { SI GNAL } \\ \text { CODE } \end{gathered}$ | $\begin{array}{cl}\text { SOURCE } & \text { AND } \\ \text { DEST } \\ \text { NATI ON }\end{array}$ | CHARACTERI STI CS AND FUNCTI ON <br> (TTL LEVELS WHERE NOT OTHERWISE stated) |
| :---: | :---: | :---: |
| PO-20 | VBD to PSD <br> $(20,27$, $(59)$ <br> $21,20)$  | 15 nsec. Derviced from PO-17 if Bust situation exist Clocks 3 decade counters on PSD for parallel load. Loads last score if LI-31 is at 0 . |
| PO-21 | WBD to GPM <br> (18 (50) | 80 nsec . Occurs when BUST detected. |
| PI-22 | WBD to LDPS <br> (43) (40) | 20 msec . Occurs when WIN situation detected. Drives RL2 on LDPS to activate gong. (Used in current sink mode, hence little voltage change if nonitored. (logic 0 typ. $0.3 v \quad$ logic 1 typ. 0.7 v ) ). |
| PO-23 | $\begin{array}{ll} \text { to WBD } \\ & 37) \end{array}$ | Not currently used. If' pulse applied to VBD wi 11 zreate a BUST situation. |
| PI-24 | $\begin{array}{cc} \text { GPM } & \text { to LDPS } \\ (19) & (39) \end{array}$ | Inverse of PO 21. Drives relay RLI on LDPS to activa Buzzer. Used in current sink node (as P1-22) |
| PI-25 | $\begin{array}{ll} \text { GPM }: 0 & \text { LDPS } \\ (61) & (41) \end{array}$ | Pul se of 5 seconds following 'player change' . Drives RLI on notherboard to change captions' illumination from 'Throw Darts' to "Remove Darts'. |
| PO-26 | LDPS to RL1 <br> (9) (MB) | Drive si gnal to RL1 resulting from Pl-25. |
|  | $\angle L O A S$ | for Blouving Fewses Change TR 22 or pances lizand (2N4059) <br>  tumyes plangers canded Ly LDPS; TR II-2NHY Od |


| SIGNAL CODE | SOURCE AND DEST NATI ON | CHARACTERI STI CS AND FUNCTI ON <br> (TtL Levels where NOT Otherm se stated) |
| :---: | :---: | :---: |
| LO. 01 | $\begin{aligned} & \mathbf{G P M} \\ & (38,36,35,1) \end{aligned}$ | Si gnal s not used |
| L1-02 | GPM to PSD $\mathfrak{i} 2,3,4,40)(54$ | Derived from ' number of players in gane' register. Drives (via PSD and out on L1-30) associ ated LED disp Used in current si nk node. |
| L1-03 | GPM to LDPS | Derived from 'pl ayers turn' register on GPM Used to |
| LI-04 | (29 " (51) | drive associated caption lamps indicating whose turn |
| Lİ-05 | (54 " (49) | it is to play. Players 1 thru 4 run in sequence as |
| L1-06 | $\begin{array}{lll}(37 & \prime \prime & (47) \\ (5) & \prime \prime & (45)\end{array}$ | L1-03 thru L1-06. Used in current sink mode. |
| LI-07 | GPM (14 UBD 29 | Derived from 'pl ayers turn' register. Used on VBD to |
| 니-08 | (15 23 | gate out pulses etc to correct PSD. |
| LI-09 | (16 22 |  |
| L1-10 | (17 19 |  |
| LO. 11 |  | Not al l ocat ed. |
| LO. 12 | $\begin{array}{ll} \text { PSD } & \text { to } \begin{array}{c} \text { VBD } \\ (50) \end{array} \\ & (16,15 \\ & 14,13) \end{array}$ | Occurs if a score exceeding 0 detected in decade coun on PSD. Used to cl ock WIN and BUST regi ster. If sco is 0 then LO-12 is a level at 0 and win register cloc If score exceeds 0 then LO 12 is a pulse 100 msec Iong and BUST regi ster clocked. |
| L1-13 | $\begin{array}{lll} \text { VBD to } & \text { LDPS } \\ (41) & & (38) \end{array}$ | Occurs when first coin is inserted and Iasts till 1 s after WN detected. Drives 'Board III umination Lamp' via RL3 on LDPS. Used in current sink mode. |
| LI-14 | VBD to LDPS  <br> (1) (43) | Occurs when $W N$ regi stered. Cancelled by insertion $c_{1}$ first coin. Drives GAMEOVER Iamp via LO 40. Used in current si nk node. |
| LO. 15 | VBD to SPC  <br>   \& GPM <br> (2) (5) $(27$  | Inverse of L1-14. Used on SPC to prevent registering further scores after a win. and stops 'player change' from working on GPM |
| Lİ-16 | WBD to LDPS | Gated output of $W N$ and which players turn it is. Us |
| LI-17 | (6) " (50) | via LO. 33, LO. 35, LO. 37, and LO 39 (and LDPS) to driv |
| L1-18 | (5) " (48) | associ ated WN caption I amps. |
| L1-19 | $\begin{array}{lll}(4) & " & (46) \\ (3) & " & (44)\end{array}$ |  |
| O. 20 | $\begin{array}{ll} \text { WBD } & \text { to } \\ \text { (12) } & \text { SPC } \\ \hline \end{array}$ | Occurs in a BUST situation. Used on SPC to prevent registering further scores in a BUST situation. Rese by ' pl ayer change' bei ng pushed. |
| L1-21 | $\begin{array}{lrl} \text { VBD } & \text { to } & \text { LDPS } \\ (11) & (42) \end{array}$ | Inverse of LO-20. Drives BUST Iamp via LO-41 on LDPS Used in current sink node. |
| LO-22 | GPM to $\left.\begin{array}{c}\text { SPC } \\ (59) \\ (19)\end{array}\right)$ | I nhi bits scoring on SPC for 5 seconds after 'player change.' has been pushed. |


| $\begin{aligned} & \text { SI GNLL } \\ & \text { CODE } \end{aligned}$ | $\begin{aligned} & \text { SOURCE AND } \\ & \text { DESTINATION } \end{aligned}$ | CHARACTERISTICS AND FUNCTIO'N <br> (TTL LEVEL WHERE NOT OTHERWISE sTAted) |
| :---: | :---: | :---: |
| LO. 23 | to PSD(4) <br> and TSD( 15 | not connected. Potential use as Lamp Test facility for al 7 segment di spl ays. |
| $\begin{aligned} & \text { LO. } 24 \\ & \text { LO. } 25 \\ & \text { LO. } 26 \end{aligned}$ | TSD to 7 seg di spl ays |  |
| $\begin{aligned} & \text { LO. } 27 \\ & \text { LO. } 28 \\ & \text { LO. } 29 \end{aligned}$ | PSD to 7 seg disp ays | units As above. The 4 PSD sources drive the <br> tens  <br> hundreds ( $F$ respective pl ayers score.  <br> segnent omitted).  |
| LI-30 | PSD to di spla '. 19 \& 51) | Derived from appropriate Ll-02. Supplies current (fr 10 V FWR) to common anode of associ ated players displa |
| L1-31 | $\begin{array}{ll} \text { GPM to PSD } \\ (39,6 & (61) \\ 7,8) & \end{array}$ | Set to 1 by inserting first coin. At 0 by either 'switch on reset' or 'pl ayer change' (PO 11) or 'firs date' (PO-01). In 1 state allows parallel entry of 301 into 3 decade co-unters on PSD. In 0 state allows parallel entry of last score as held in display regi ster. |
|  | - DPS to captio |  |
| LO- 32 | 19) " lamps |  |
| LO. 33 | 18) " | " <br> win |
| LO. 34 | 17) " | Pl ayer 2 |
| LO- 35 | 16) " | ${ }^{11}$ win |
| LO-36 | 15) " | Pl ayer 3 |
| LO. 37 | 14) " | " win |
| LO-38 | 13) " | Pl ayer 4 |
| $\text { LO } 39$ | 12) " | " win |
| $\text { LO. } 40$ | 11) " | Gameover |
| LO. 41 | $10)^{\prime}$ | BUST |

5. 3 The Score-to-Pul se Conversion (SPC) Card (PL1) on Mbther board)

The 6 encoded inputs PO 01 through PO. 06 (wei ghted 1,2,4,8,16,32 respectively) from the dartboard and its diode natrix are the prime inputs to this card. Because of the non uniform nature of the dartboard signal, each of these six are conditioned into uniform pulses, around 50 miliseconds long, by nonostables (IC's 3,2,6,1, 4, and 5 resply).

The outputs of these nonostables are- clocked into registers IC7 and IC9 by means of a clock pulse from IC11. This clock pulse can be inhibited by LO 15 and LO 20 and these are used to prevent a score registering in the case of $a \operatorname{win}$ or bust.

When a score is made, IC20, a 10 KHz oscilletor is gated to start. Pul ses from it fill up a counter, (IC16 and IC14) and when the number in it is the same as the score, then a bit comparator (IC15 and IC19) stops the oscilletor.

Pul ses are out put from this card on pins 15 and 17 as P1-08 and Pl -09. Only $\mathrm{P} 1-09$ is used and is routed to the GPM card.


5. 4 The Gane and Pl ayer Managenent (GPM card (PL2) on the Mbtherboard)

The maj or function of this card are:
(i) to count the number of coins and hence the number of players in the gane. to sequence the players' turn when the player change button is pressed to distribute the score pulse train (from the SPC card (PO-09) to the appropriate PSD card). to reset the gare to a GAMEOVER' condition with power on.

The pulse from the coin mechani sm P0-10, triggers a nonostable IC12 which clocks a 4 bit shift register IC18. With suitable buffering, the 4 outputs of this register leave the card as LO 02 (a) through (d) and are routed to each PSD card. (There they allow currents to pass through the players score LED s). Pin 6 of IC18 is a 'mode control' input and will allow IC18 to shift right or to have a parallel input. The parallel input is 1000 and occurs when the first coin is inserted (see sect 2.4). A register, IC19, controls this, it being set by a 'player change' signal (PO 11) or by the nachi ne being powered up. It is cleared by the coin mechanism pulse.

Operation of the 'player change' button will trigger a 5 second nonostable, IC24 which, if LO 15 is a logic 1, will trigger monostable IC22. During this 5 second del ay, signal LO-22 inhibits scoring as the SPC card and signal Pl-25 operates, via a rel ay driver circuit on the LDPS card, RLI on the Mbtherboard. (This controls the caption' lamps, changing THROW DARTS to REMDVE DARTS as the illum nated caption for the 5 seconds).

IC22 output is or-ed with the coin mechanism pulse in IC6 gate 1 and buffered in IC3 gate 1 to give PO.17. This pulse feeds the UBD card to reset the BUST register. This out put from IC6 gate 1 also is used as the clock for a second 4 bit shift register, IC11. The conbination of gates using IC's 16 and 20 and parts of IC's 15, 4 and 17 control the ' node control' input of IC11. Essentially they allow a parallel entry of 1000 for the first player and then a shift right every time the 'player change' is pushed. If 2 players are playing, IC11 cycles through 1000, 0100, 1000,0100 etc. If 3 pl ayers are playing it cycles 1000, 0100, 0010, 1000, 0100, 0010 etc. and for 4 players it cycles 1000, 0100, 0010, 0001, 1000 etc. from IC11 via suitable buffering LI-07 through L1-10 are output to the VBD card to signal which player is taking his turn and L1-03 through LI-06 is output. These letter 4 drive, via I amp drivers on the LDPS card the caption lamps indicating whose turn it is.

| MTL \# | NO. OFF | CCT. REF. | DESCRIPTION | SUPPLIERIORDERING INFO |
| :---: | :---: | :---: | :---: | :---: |
| \#053 | 3 | IC $2,7,8$ | SN-7400 | tti integrated circuit |
| 054 | 2 | IC 1,3 | SN-7404 |  |
| 055 | 5 | $\begin{gathered} \text { IC } 4,5,9, \\ 10,13 \end{gathered}$ | SN-7420 |  |
| 059 | 1 | IC 11 | SN-7474 | " |
| 064 | 5 | $\begin{gathered} \text { IC } 6,12,14 \\ 15,16 \end{gathered}$ | SN-74121 | 11 |
| 010 | 1 | R7 | $100 \Omega$ | RESISTORS-GENERAL PURPOSE $10 \%, 1 / 4 \mathrm{~W}$ |
| 027 | 1 | R6 | $1.8 \mathrm{~K} \Omega$ | " |
| 028 | 1 | R3 | 2.7 Kg | " |
| 029 | 1 | R4 | 5.6 Ke | 11 |
| 024 | 1 | R2 | $10 \mathrm{~K} \Omega$ | 11 |
| 031 | 2 | R1,5 | 22 Ks | " |
| 001 | 11 | $\begin{gathered} \text { c } 2,3,5,6, \\ 7,9,10,12 \\ 15,16 \end{gathered}$ | 0.01MF, 25 V | CAPACITOR, MONOLITHIC CERAMIC <br> -RADIAL LEADS <br> -TEMPERATURE CHARACTER. NOT CRITICAL <br> -TYPICAL TOLERANCE $+80 \%,-20 \%$ |
|  |  |  |  |  |
|  |  |  |  |  |
| 002 |  | c8,11,13,14 | $\begin{gathered} 5 \mu \mathrm{~F}(\mathrm{OR} 4.7 \mu \mathrm{~V}) \\ \mathbf{2 5 V} \end{gathered}$ | CAPACITOR, MIN. AL. ELECTROLYTIC |
|  |  |  |  | - AXIAL LEADS |
|  |  |  |  | -TEMP. CHARACTERISTJCS NOT CRITICAL |
|  |  |  |  | $\begin{gathered} - \text { TYPICAL TOLERANCE } \\ +100 \%,-20 \% \end{gathered}$ |
| 003 | 1 | Cl | 10, F 25V TYP. |  |
|  |  |  |  | " |
| 005 | 1 | c4 | $50 \mu \mathrm{~F} 25 \mathrm{~V}$ T Y P. | 11 |
|  |  |  |  |  |
| SP504 |  |  | WBD CARD |  |
|  |  |  | ( Compl ete | enbl y) |

The WN and BUST Detection (VBD) card. (con't)

The second register of IC11 is the BUST register. It outputs L1-20 to the SPC card to prevent any further scoring and L1-21 to the LDPS card and thence to the BUST Iamp. It also triggers nonostable ICl5 which provides a pulse to drive the buzzer.

The pulse from IC15 is also used with gating from the appropriate 'player turn' signals (L1-07 to 10) to produce $P 0-20$ a through d. These are routed to the 4 PSD cards and become clock pulses to effect:- parallel load of the 3 decade counters. (In a bust condition they are loaded with the players last score).

Pul se PO 17 is fed from the GPM card to this cardrand is used to trigger nonostable IC12 and reset the Bust register. (This monostable is al so triggered by the $W N$ register being set). The resultant pulse from IC12 is gated with the inverted output of the Bust register and the previously mentioned 'players turn' signals (LI-07 through 10) to produce PO-19 a through d. PO 19 is routed to the PSD cards and clocks into a 3 decade register the players current score. Hence when a player has notbusted then his 'last' score is updated. PO-19 is al so generated in a wincondion such that the winning ayer has a presented score of zero.
5. 6 The Pl ayers Score and' Di spl ay (PSD) card
( Pl ugs 4,5,6 and 7 on the Mbtherboard)
A three decade counter, IC's 6, 10 and 9 (units, tens and hundreds respectively) is fed by a pulse train P1-18 from the SPC card. The out put from this counter feeds 3 bi nary-to-7 segnent display decoders (IC's 2,3 and 5) whose outputs are taken in turn to LED's on the Mbtherboard.

IC's $12,13,14,15$ and 16 are multiplexes whose output.is controlled by LI-31. Their outputs feed the 3 decade counter and with LI-31 at a (which occurs at the start of a gane) and PO-15 occurring, 301 is I oaded into the counters. With LI-31 at a 0 and PO-20 occuring then the players last score is loaded into the counters. (This is the result of a BUST condition).

Pulse PO-19 is derived from the UBD card and loads the players I ast valid score into IC's 1,8 and 4 when he has finished his turn and he has not bust.

Si gnal L1-02 turns on TR1 and TR2 to supply the players LED score displays with current so that only those players who are taking part have thei $r$ di spl ays illuminated.

| MTL\# | NO.OFF. | CCT.REF. | COMPN. TYPE | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: |
| \#053 | 1 | IC 11 | SN-7400 | TTL INTEGRATED CIRCUIT |
| 054 | 1 | IC 7 | SN-7404. | " |
| 057 | 3 | Ic 2,3,5 | SN-7447A | " |
| 058 | 5 | $\begin{aligned} & \text { i c } 12,13,14, \\ & 15,16 \end{aligned}$ | SN-7451 | " |
| 060 | 3 | IC $1,4,8$, | SN-7475 | " |
| 066 | 3 | IC 6,9,10 | SN-74192 | " |
| 095 | 20 | RI THRU R20 | $390 \Omega$. | $\begin{aligned} & \text { RESISTOR- GENERAL SUPPLY } \\ & 1 / 2 W, 10 \% \end{aligned}$ |
| 028 |  | R22 | 2.7 Ke | RESISTOR $1 / 4 \mathrm{~W}, 10 \%$ |
| 030 | 2 | R21,23 | 10K | " " |
| 003 | 1 | C I | 10MF, 25 V т Y p. | CAPACITOR, MIN. AL. ELECTROLYTIC |
|  |  |  |  | -AXIAL LEADS <br> -TYPICAL TOLERANCE |
|  |  |  |  | $+100 \%,-20 \%$ |
| 001 | 7 | C2 THRU C8 | 0.01 $\mu \mathrm{F} 25 \mathrm{~V}$ | CAPACITOR, MONOLITHIC CERAMIC <br> -RADIAL LEADS |
|  |  |  |  | -TEMP. CHARACTERISTICS <br> NOT CRITICAL <br> -TYPICAL TOLERANCE $+80 \%,-20 \%$ |
| 040 | 1 | TRI | 2N3708 (TI) | TRANSISTOR -SI, N-p-N, PLANAR |
| 042 | 1 | TR2 | 2N4402 (м о т) | TRANSISTOR -SI, P-N-P, MED. CURRENT $\begin{aligned} & -V_{C E}=30 \mathrm{~V} \\ & -I_{C}=1 / 2 \mathrm{~A} \text { TYPICALLY } \end{aligned}$ |
| 096 | 1 | - | HEATSINK FOR \#042 (TR2) | $\begin{aligned} & \text { TO-92 HEATS INK } \\ & \text {-RCA TYPE KM } 3413 \end{aligned}$ |
| SP505 |  |  | PSD CARD |  |
|  |  |  | ( Compl ete | senbl y) |

## 5. 6 The Lamp Driver and Power Supply (LDPS) card

 ( PL8 on the Mbther board)The I amp driving parts of this card consist of 10 identical circuits (T1 through T10 and associated components) which have a drive capability of 500 mA . The specific lamps they drive are detailed el sewhere (notably in the signal description lists).

Four further circuits, identical except for the addition of a single suppression di ode across the drive transistor, (T11 through T14 and associ ated components) are rel ay drives. Three rel ays are nounted on this card and the fourth is on the Mbtherboard, as RL1, and controls the illumination of the 'Throw Darts! and ' Renove Darts' captions.

The +5 volts power supply regulator is an amplifier consisting of T21,20,19,17 and 18 in that sequence. The latter being the out put transistors and are mounted on the heatsinks. Adj ust ment to the 5 volts is made by RVI, an anticlockuise novement of which will increase the voltage. The stability of the 5 volt supply is determined by the reference voltage derived from D12 and D13 circuitry and will maintain the output within 50 milivolts from no load to 4 amps.

Overcurrent protection is provided by the circuitry around T15 and T16. Nornally those are off and only when the current through R17 and R33 is sufficiently high to cause the voltage drop across R17/33 to exceed about $2 \frac{1}{2}$ volts will T15 and T16 conduct. Once conducting they latch thensel ves on and cause T17 and T18 to be hel d OFF. Onl $y$ by disconnecting power from the nachi ne for about 5 seconds and then reconnecting will the power supply circuit be reset for nornal operation.

Over voltage protection is provided by the 'crowbar' circuit T22 and SCR1. Normally there are OFF but if the monitored voltage, the 5 volt line, rises to around i-5.5 volts then T22 will conduct and five SCR1. Having fired, the 5 volt line is pulled down and either the overcurrent protection circuit will trip or fuse FSI will slow.

A further snall overvoltage protection for very fast transients is provided by zener di ode 015 of $\mathbf{5 . 6} \mathbf{~ v o l t s , ~ w h i c h ~ i s ~ s t r a p p e d ~ a c r o s s ~}$ the 5 volt line.

| M TL \# | NO.OFF | CCT.REF. | COMPN. TYPE | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: |
| \# 041 | 14 | TI THRU TI 4 | $2 \sim 4400$ (TI) | $\begin{aligned} & \text { TRANSISTOR }-N-P-N, \text { SI } \\ & \text { PLANAR } \\ & -V_{C E}=30 V \\ & -1, ~ I A P E A K \\ & -T U 5 O R \text { TO92 CASE } \end{aligned}$ |
| 043 | 3 | T15, T20, T22 | 2 N 4059 (TI) | $\begin{gathered} \text { TRANSISTOR-P-N-P, } \quad \text { SI } \\ \text { PLANAR } \end{gathered}$ |
| 040 | 3 | T16, T19,T21 | 2 N 3708 (TI) | $\begin{array}{rl} V C E & 30 \mathrm{~V} \\ - \text { IC } & =200 \mathrm{MA}, \operatorname{TO92} \text { CASE } \\ \text { TRANSISTOR-N-P-N SI } \\ & \text { PLANAR } \end{array}$ |
|  |  |  |  | $\begin{aligned} & -V_{C E}=30 \mathrm{~V} \\ & -I=200 \mathrm{MA} \\ & -T C 92 \text { CASE } \end{aligned}$ |
| 044 | 1 | T19 | TIP 31 (TI) | TRANSISTOR- NPN SI POWER $-V_{C E}=40 \mathrm{~V}$ <br> $-T=3 A$ <br> - TO 220 AB CASE |
| 045 | 1 | T18 | $2 N 3055$ | TRANSISTOR-NPN SI POWER $-V_{C E}=60 \mathrm{~V}$ <br> $-I_{C}=10 \mathrm{~A}$ <br> -METAL CAN TO3 CASE |
| 048 | 4 | D1, D2, D3, D16 | IN 4001 | $\begin{aligned} & \text { DIODE - SI RECTIFIER } \\ & -1=1.5 A, V_{\text {PIV }}=50 \mathrm{~V}, \\ & -D \& 41 \text { CASE } \end{aligned}$ |
| 049 | 6 | D4 THRU D9 | IN 1200 | DIODE - SI RECTIFIER $-I_{F}=10 \mathrm{~A}, V_{P I V}=10 G \mathrm{~V}$ -STUD ROUNTING <br> CASE |
| 047 | 2 | D11, D13 | IN 4148 | DIODE - SI SIGNAL |
| 050 | 1 | D14 | IN 751A | $\begin{aligned} & \text { DIODE -ZENER } \\ & -V_{Z}=5.1 \mathrm{~V} \\ & -\mathrm{P}=400 \mathrm{MW} \end{aligned}$ |
| 051 | 2 | D 12 , DIO | 1 N 746 A | $\begin{gathered} \text { DIODE -ZENER } \\ -V_{Z} 3.3 \mathrm{~V} \\ -P=400 \mathrm{MW} \end{gathered}$ |
| 052 | 1 | D 15 | IN 752 A | $\begin{gathered} \text { DIODE }-Z E N E R \\ -V_{Z}=5.6 \mathrm{~V} \\ -P=400 \mathrm{MW} \end{gathered}$ |
| 046 | 1 | SCRI | $\begin{array}{ll} \text { TIC } 106 \mathrm{~F} & (\mathrm{TI}) \\ \mathrm{Cl} 22 \mathrm{D} & (\mathrm{GE}) \end{array}$ | $\begin{aligned} & \text { SCR } \\ & -I=5 A, V \\ & -T E 220-A B P C X=50 v \end{aligned}$ |
| 039 | 1 | LED 1 | $\begin{aligned} & R L-4850(L I T) \\ & 5082-4850(M P) \end{aligned}$ | LIGHT EMITTING DIODE |
| 035 | 1 | R 25 | $82 \Omega$ | RESISTOR--GENERAL PURPOSE |
| 010 | 2 | R30, R31 | $100 \Omega$ | $10 \% .1 / 4 W$ |
| 011 | 1 | R 27 | $180 \Omega$ | 11 |
| 012 | 2 | R28,R32 | $220 \Omega$ | 11 |


6. 1 Machi ne 'Dead'

If the Iamps behi nd the 'Player Change' caption are not lit then this indicates a lack of power to the nachi ne.

Check--preferably in this order:
(i) the main outlet socket supplying the nachi ne and any extention cord if one nay be used. A significant number of ' nachi ne' faults are attributable to a lack of 115 V ac. plug 9 is correctly nated with the Mbtherboard (PL 9 is the 18 way pl ug interfacing the cabi net cabl ef orm to the electronics package and is at the left hand edge of the notherboard.)

If the Iamps behind the 'Player Change' caption are lit but no scores are indicated and no other captions are lit, then probably the protection devices on the power supply have been triggered.

Check the smal LED Iamp on the top of the LDPS card (the one with the big heat sink attached). If it is not lit then unpl ug the machi ne- WA T 5 SECONDS- and pl ug it in. (This del ay allous the protection circuitry to reset itself.)

Mbst nachi nes have-this power supply card fixed to the aabi net by means of a steel bracket. However if the machi ne doesn' $t$ have this, then occasionally the power supply card works its way loose. Check therefore that it is uell located in its connector.
NOTE: The 5 amp fuse on the Power Supply is not in the nain circuit. It is only protection for the 5 volt line.
6. 2 Machi ne 'live' but not recognizing coins

Look first at the coin mechani sm and check that the coins pass properly past the microswitch. A paragraph on the care and cleani ng of this nechanism will be found in Section 7.

Failure of the microswitch to put up players may be traced to the 3 pin plug connecting the upper and lower cabi nets not being properly mated. A further check can be made at Plug 9 at the Ieft hand side of the Mbtherboard. With a short length of bare-tinned copper wire, carefully short together pins 1 and 2 of PL9 when it is connected in circuit. This will simete the action of the microswitch.

If this last test works then a faulty microswitch has been identified. If it still fails to put up players then replace the GPM card.
6. 3 Machi ne giving more than one player per coin

Mbst machi nes have a 100 ohm resistor connected in series with the coin mechani sm microswitch contacts and the electronics. This together with C21 on the GPM card forns a filter which only allous pulses of the right duration corresponding to coins passing the switch. Hence vi olent hitting of the front of the coin door, although it will cause the snap action microswitch to jump over and make momentary contact, will not put-up 'free' games.

Where the occasion arises that one coin will put up tho players then the GPM card has to be replaced. It is often a failure of IC18 on this card which causes this fault.
6. 4 Machi ne not scoring properly

This can be caused by faults in the el ectronics or problens, with the Dartboard Assenbly and the technique is to ascertain whi ch of these two are gi ving trouble.

Set up 4 players in a new gane and score a single 13 for each. (Take care not to hol down the 13 segment too long so that it could be recorded twice over).. Check the displayed score reads 288 for each.

If one of the segments of a di splay are missing, for instance it could read 280 if the middle bar of the units was not lit, swith off power and exchange that $p l$ ayers PSD card with anothers and repeat' the test.

If the fault 'follows' the PSD card then the card is faulty and needs replacement. If the fault stays in the same position then the display needs replacing. The replacement proceedure is outlined in section 6.11

After checking the displays, di sconnect the Dartboard from the Mbtherboard by renoving PL10 from the Mbtherboard. Pl ug Test Assembly TA 000 into the PL10 position on the Mbtherboard.

VIth a pl ayer up on the machine, operation of TA 1000 should gi ve a score of 63 points. (This will be 63 points deducted from whatever score that player started with for example if -he started at 301 the new score woul d be 238).

A correct indication that 63 points have been scored confirns that the electronics is good and it is the dartboard which has the fault. In either case renove the si mul ator and reconnect the dartboard.
6.4a Dartboard mis-scoring

Each segnent on the dartboard has a score val ue which is encoded into a bi nary code for the el ectronics to recognize. The code consists of the numbers $1,2,4,8,16$ and 32 and each score is broken down into a uni que combi nation of these numbers. A score of 20 will therefore activate the 4 line and the 16 line and a score of 5 will activate the 1 line and the 4 line.

If by a del iberate action the single 5 and single 20 were to be pressed si multaneously, the numbers 16,4 and 1 nould be activated. (The 4 Iine although appearing in both can only be activated once.) The el ectronics will recognize these numbers and register the sum of them - which is in this case would be 21.

With this prior expl anation of the encoding techni que the process of deducing the location and type of fault on the dartboard can be undertaken.

Three types of fault are predictable on the dartboard assembly: - an oversensitive switch or even a switch that is al ways closed, -an undersensitive switch including one that never makes contact, - a bad di ode on the 'wrap around' di ode matrix.

Assuming that only one fault is present the procedure is one of el i mi nation.

## 6.4a Dartboard mis-scoring (con't)

Press in turn, and taking note of the recorded score at each time, the segments: singles $1,2,4,8,16$ and double 16.

If any of these numbers fail to record, note the ones which are bad, add these missing numbers together and investigate those switch contacts (for pernanently made contacts) whose val ue is this sum total of missing scores. (lt is best to repeat this proceedure to confirm that a missing score is not caused by an undersensitive switch on one of those segments pressed). A pernanently closed contact on one of the switches will prevent any of those Iines to which it is connected from being recognized. Assume that the single 9 switch is sufficiently out of adjust nent such that it is al ways closed. This will tie down the 8 and the 1 iine. Adopting the proceedure outlined above whereby the $1,2,4,8,16$ and double 16 segments are pressed, onl $y$, in this case, the 2,4,16 and "32" will be shown. The 8 and 1 are missing indicating that a segment with a score of 9 is causing trouble.

A number of the segnent switches are tied together where their scores are the same. Typically triple 3 is tied to single 9. This linking is done on the natrix board. Care should therefore be adopted in following the checkout proceedure outlined above in case there may be more than one switch tied to that line.

Ret urning to the example gi ven, with an 8 and a 1 missing it could be either of the tuo single 9 segnent suitches or the triple 3 segnent switches. Careful examination will rapidly identify the fault.

Obt ai ni ng correct indi cations of $1,2,4,8,16$ and 32 will eliminate
the possibility of permanently closed switches.
The next stage of the elimination process is to press each segment in turn to check that they are neither supersensitive, in which case the blades of the switches should be eased apart, nor undersensitive, in which case the blades should be noved closer.

If a segment fails to score even with the contacts closing then cleaning the contacts with a paper towel noistened with a mild sol vent should be tried.

If one of the encoding di odes in the ' wrap-around' natrix board has become open circuit then its component of the score will be missing. Again an exampl e: single 15 comprises $1,2,4$ and 8 . If the di ode to the 2 line is open circuit the score will be encoded at 1,4 and 8 gi vi ng 13.

The six encoded 1 ines from the matrix passimmediately into the SPC card. The SPC card converts the score into a pulse train which is fed to one of the four PSD cards. depending upon whose turn it is. The majority of mis-scoring problens in the el ectronics is theref ore in the SPC or the PSD cards.

The proceedure to narrow down the fault identification is recommended to be:
(i) put four players up on-the ma-chine with number 1 player up activate the bad score
put player 2 up by pressing the player change, button and agai $n$ score the affected-score
(v) if the ba if the bad score was only on one of the 4 players score then that players PSD - card is-suspect. Switch off power, exchange the suspect card. with a good one al ready in the machi ne and go through the above proceedure againt. if the fault 'follows' the PSD card then it i-s definitely that PSD card which is faulty.
if the fault stays in the same jocation after shifting the PSD cards around then the-GPM card needs replacing.
为
6. 5 Machi ne not ei ther $W$ nni ng, or Busting, or Both

In the el ectronics package, si gnals from all 4 players score cards (PSD) feed the $W$ n and Bust Detection card. If theref ore only one player is experiencing difficulty in winning or busting it could be his PSD card or the VBD card. The answer is ascertained by switching off the machi ne and suapping the suspected PSD card with a good one and repeating the test. If the fault is still in that same position, the VBD card is at fault but if the fault follows the PSD card then it is the PSD card at fault. Repl acenent of the appropriate card is the cure.

After detecting that a pl ayer has won or bust the UBD card activates a number of caption lamps etc. These are not driven directly from the VBD card but go through lamp or rel ay drivers on the power supply card (LDPS). For instance Pl ayer 2's WN I amp nay fail to cone on when he wi ns but the gane nay show 'GAMEOVER'Iit, the gong activated and the Board IIIumination Lamp turned off. This could be caused by the lamp itself burning out and needing replacing, or the Iamp driver circuit on the LDPS card not operating or the appropriate signal not coming out of the VBD card. Sel ective repl acement of each card in turn uould identify the cause of the problem

Similarly for gong and buzzer problens. A failure of either of these nay be caused by the component itself not functioning properly or the rel ay and driver on the LDPS card or the appropriate si gnal s from the VBD card.
6. 6 Machi ne not changing pl ayers

The player change push button feeds only into the GPM card. Problens therefore with the machine not changing players concern only these rel ated itens.

Check first that the push button is making proper contact. As the body of the swith is transparent and al so renovable from the 'pusher' this can be accomplished. The two wires from the player change puch button enter the notherboard on PL10 pins 3 and 4. Check theref ore that this pl ug is fully nated. Substitution of the GPM card by one that is known to uork is the renai ning action necessary to identify the location of this fault.
6.7 Machi ne not changing players snoothly

This is al nost invariably a problem on the GPM card. Substitution of the existing GPM card by another wili effect a cure.

The nost likely source of this problem on the GPM card is IC24 and IC22.
6. 8 Machi ne not switching bet ween 'Throw Darts' and 'Renove Darts'

The Pl ayer Change pushbutton initiates this sequence whereby for 5 seconds after pressing it, the dartboard is de-activated (so that players can renove their darts without giving thensel ves false scores) and the 'Throw Darts' caption goes out and the 'Renave Darts' caption cones on. After 5 seconds the machine reverts to its normal node.

The rel ay PLI on the Mbtherboard (lover I eft hand side underneath Cl) controls these 2 caption lamps. They are supplied with 115V ac and are 3 watt bulbs. The rel ay when going over will give quite an audible 'click' and can be heard from the front of the nachi ne. If no 'click' is heard than the GPM card nay need changing. If a 'click' is heard then probably one or both of the bul bs need repl aci ng.
6. 9 Machi ne not locked out after switch on.

The nachi ne is desi gned to set ' GAMEOVER' upon first appl yi ng power. In this condition no scores will be recognized and the pl ayer change push button will have no effect.

After switch on and before any coin is inserted, the only guaranteed caption lamp to be on will be this 'GAMEOVER' I amp. If this is not on and if the nachine can be played without a coin being inserted then the GPM card uould need repl aci ng.
6. 10 Machi ne not locked-out after Bust and Vīn

The nachi ne will not recognize any scores when a player has bust or non. Until either in the case of a bust, the player change pushbutton is pressed or in the case of a WN a coin is inserted. If either of these conditions are not being net then the GPM card would probably be at faul.
6. 11 Repl acenent of a faulty 7 segnent LED score di splay

A rapid check of all the segments on the 4 players score di spl ays is to set the nachi ne to 4 players and score 13 for each. This will present a score of 288 and in this condition all the segments are driven and missing one is immedi ately apparent.

Switch off power and renove the 8 printed circuit cards from the Mbtherboard. Di sconnect the two connectors at either end of the Mbtherboard and renove the $8 \frac{1}{2} "$ screns fixing it to the cabi net.

Using a sol der sucker and a temperature controlled soldering iron, renove the solder from the legs of the faulty display and then gently ease the display from the notherboard.

Repl ace with a display of a matching type and check after soldering that no sol der splashes or bridges are present.

Repl ace the notherboard in the cabi net using the reverse proceedure outlined above.
6. 12 Repl acement of a caption I amp.

Use the proceedure given in section 6.11 for the renoval of the motherboard and after its renoval, extract the dead lamp.

The repl acenent lamps cone supplied with sockets on their 2 leads. There should be discarded, the leads bent over and the lamps inserted such that they point UP if they are on the upper half of the notherboard and DOWN if on the lower half.

Repl ace the notherboard and check the machi ne for proper oper at $i$ on.
7. 1 The Coi $\mathbf{n}$ Mechani sm

Periodically clean the mechani sm by using a screw driver with a cl oth over the blade of the screw driver. The mechanism must be free of any foreign natter which may cushi on the bounce of the coin.

Keep all magnets clean of all foreign matter. When ever necessary, the accept or should be cleaned with hot uater and a cleanser. The steps are as follows:

1. Place accept or in boiling water and allow to soak for about 10 min .
2. After soaking, use a brush and kitchen cleaner to clean foreign
natter.
3. Again, rinse in boiling water.
4. Dry throughly by using filtered compressed air.

NOTE: Hot water is recommended as it evaporates rapidly and speeds the drying process.
5. Use poudered graphite on onl $y$ the noving parts of the acceptor.

Use care to keep the pondered graphite away from the paths that
are followed by the coins. DO NOT USE OIL.
7. 2 The Dartboard Assenbly

The occasi onal adjustment of the switches to ensure that each segment has the same sensitivity as all the others. The procedure outlined in section 6.4a where problens of mis-scoring with the dartboard, is applicable here for proper switch alignment.
7. 3 The El ectroni cs Package

As all. the controls are perforned by digital logic there is no adjustments or maintenance required in this area.

At each service call all this is required is to ensure that all 8 cards are firmy located in their sockets and have not norked loose.

On the LDPS card there is a snall potentioneter which has been factory set and locked into position. This presets the control power supply at +5 volts. Providing that this supply is within 4. 75 volts to 5. 25 volts then no adjustment is necessary. If this voltage is to be nonitored then an accurate dc voltneter can be connected across' Cl of any of the 7 Iogic cards.

### 7.4 The Buzzer

Adjusting the lower fixing screw of the Buzzer mounting plate controls the vol une of the buzzer. It needs to be screwed in so that the head of the fixing screw of the buzzer itself just lighty rests agai nst the cabi net,
7. 5 The Servicenans Kit

The following itens will be necessary as particular needs to this machine. A normal complenent of screudrivers, wrenches, wire, etc. is assuned to be al ready a part of the kit.

Speci al Tool s
$--7 / 16^{\prime \prime}$ open ended urench for the renoval of the dartboard
--temper at ure controlled sol dering i ron
--solder sucker
-- Dartboard si mul at or MTL\#TA 1000
Spare Parts (for 1 kit)
--SPC card (10ff) MTL\#SP 502
-- GPM card " MFL\#SP 503
-- VBD card " MR\#SP 504

- PSD card " MFL\#SP 505
--LDPS card " MR\#SP 506
--7 segment LED di spl ays (red or green as appropriate) (60ff) MR\# 080
--12 volt caption Iamps (60ff) MR\# 070
--Rel ay (RL1 on Mbtherboard) (10ff) MTL\# 099
- 115 V 3 Matt Iamps
lamps
(20ff) ML\# 257
-- Buzzer
-     - Gong
-- Bul bs for Board III umination. Lamp ( 20 ff ) Mr\#\# 258
-- Coi n Mechani sm (accept or) (10ff) MFL\#SP 509
--Switches for Dartboard contacts (100ff) MFL\# 208
(iii) Optional Itens
--Dart Tips 50 MrL\# 247
-- Compl ete Darts 10 MrL\#SP 517

ARACHNID, INC.
2500 North Main Street
Rockford, Illinois 61103

November 30, 1978

Re: Changes for new Motherboard by $P \& P$ Design
-(1) Etchwork on backside of Motherboard (blue) is much too close to I.C. pads.
-(2) Plated through holes, parallel etch work too close together for diameter of hole used.
(3) Should have plated through hole on connector edges.
$\mathscr{A}$ (4) Capacitors Cl \& C3 are electrolytic; holes are set for disc ceramic, paper.
(5) No holes for Cl5 (schematic), electrolytic.
(6) No holes for C30 (schematic), electrolytic.
(7) R144 is etched to -5 Volt, schematic calls for pull-up to Vss.
(8) Use single etch run from junction of pins $18 \& 19$ of I.C. $\$ 23$ to junction of R4 \& C40.
(9) Q35's collector is open, L7 * L8 are tied to Q35's base.
 to Vss should be no connection. Notice that $Q 51$ is mounted one
set of holes too high. Move R129 from pin 6 to pin 5.
(11) Mounting eyelets around I.C. \#40 are set too close together, R119 much too close to each other, C34 eyelets appear to be set for a disk capacitor, much too close for the electrolytic 25 microfarad that we use.
(12) R58 to R70 even, eyelets are to close together for 2 watt resistors, eyelets are set too close to LED - seven segment displays, had to mount resistors on backside of board, they belong on the topside front of board.
(13) Install 220 ohm resistor, $\frac{1}{4}$ watt onto coljector Q5l in series.
(14) c29, 33, 41 eyelets are set for disks, these capacitors are electrolytic, therefore eyelets are set too close together.
(15) Q42 is underneath L21 - move Q42 to left enough to clear L21 when folded down against board.

Changes for new Motherboard by $P \& P$ Design（Page 2）
（16）Connect $V_{S S}$ toC7
Break R9 from $V_{S S}$ and tie to VDD
Tie pin $\# 2$ of IC $\# 6$ to pin $\# 5$ of IC $\# 8$
Tie the output of IC $\# 8$ pin 6 to IC $\$ 47$ pins $13,2,4$ and IC \＃＇s $35 \& 36$ pins $13,2,10$
（20）On parts layout sheet IC $⿰ ⿰ 三 丨 ⿰ 丨 三 八 7$ is a 7405 ，schematic calls for 7408
（21）Tie pin 9，IC $⿰ ⿰ 三 丨 ⿰ 丨 三 八 7$ to pin 5，IC $⿰ ⿰ 三 丨 ⿰ 丨 三 ⿻ ⿻ 一 𠃋 十 𠃌 八 5$
（22）Tie junction R1－0 and R99 to base Q29
（23）Data Bus Line $\emptyset 3$ should be tied to the buffer IC $⿰ ⿰ 三 丨 ⿰ 丨 三 一$ 29，pin 8.

（24）Connect VCC and ground to IC＇s $\$ 24 \& 25 \& 41$
（25）Connect pin 10，IC $⿰ ⿰ 三 丨 ⿰ 丨 三 ⿻ ⿻ 一 𠃋 十 一 ~ 25 ; ~ t o ~ p i n ~ 3, ~ I C ~ 41 ~$
（26）IC 111 reverse the etchwork on pins $1 \& 2$ ，pin 1 is the input and pin 2 is the output

（28）Data Bus Line Øo not connected．Tie IC $⿰ ⿰ 三 丨 ⿰ 丨 三 八$（ 29 pin 12 to pin 2 of IC＇s 42，44，46， 48 and 50
（29）Pin 3 of IC $\# 44$ has been falsly tied to pin 7 of same XC． Schematic calls for IC $\# 42$ to be tied that way
（30）Data Bus $\emptyset_{1}$ is not connected．Tie IC $\# 29$ pin 2 to pin 3 of IC＇s 44，46， 48 and 50
（31）Tie R114 to collector of $Q 46$ to drive LED decimal points
（32）IC $\# 45$ pin 5 should be connected to IC $\# 42$ pin 10 ，and not IC $\$ 50$ pin 10

\#13 of $\mathrm{IC} \| 21$ should not be tied to pin 10 of IC $\# 21$.
IC $\% 19$ is iabeled incorrectly.
Pin $\# 10$ oile:i should be tied to pin \#6 of IC $\# 22$ and pin
$\# 2$ of $1 C \geqslant 20$. Pin $\# 10$ of $I C \# 17$ should not be tied to pin
\#1 of IC \#I7
Conmect pin $\# 8$ of IC $\# 28$ to $-5 v$
（37）C36－make it a 5 if electrolytic like the breadboard， set holes accordingly

（39）Tie pin $\# 7$ of IC $\# 37$ to $-5 v$

（41）Tie IC $\# 22$ pin $⿰ ⿰ 三 丨 ⿰ 丨 三 11 ~ t o ~-5 v ~$
（42）Tie collect Q45 to L21
（43）Reverse etchwork on IC \＃48 pins 非＇s $9 \& 10$ ，pin $\# 9$ should be tied to IC ii43 pin $\# 5$ ；pin $\# 10$ should be tied to IC $\prod_{4} 4$ pin \＃11
（44）Change value of R142 from 680 to 100 ohm
（45）Tie L5 between Q 34 coll，and $V_{2}$
（46）Tie IC \＃29 pin \＃8 to IC＇s $⿰ ⿰ 三 丨 ⿰ 丨 三 八 42,44,46,48,50$ pins $\# 7$
（47）Tie etch from R46 to LED＇s ii＇s 13，14， 15 pins 812 not pins $⿰ ⿰ 三 丨 ⿰ 丨 三 4$
（48）Tie IC $\# 40$ pin $\# 14$ to $V_{\text {CC }}$
（49）Redesign counter logic for the Remove Darts and Game Select lights．The Coin O．S．should not stop the Game Select strobe． The Remove Darts latch suppiy is being sunk by a NAND driver． These logic levels should be gated．
（50）IC $\# 42$ pin $\# 3$ should be part of Data Bus Line $\emptyset_{1}$ ．Why was it tied to Line $\emptyset_{3}$ ？
（51）Install hysterises buffers on inputs from dartboard

$53 j$

## TEST PROCEDURE LDPS BOARD

-NTH LIPS TEST SET-

## TEST NUMBER

## TEST ROUT NE

1. $\quad$ a. Check vi sually that no joints are unsold cered or look cold and that there are no sol der spl ashes.
b. Apply serial number to card, with permanent marker.
2. 

Use ohm meter to check for good insulation between heat si mk and the cases of all components mounted on it.
3. a. Turn RV 1 fully clockwise se.
b. Insert 5 Amp fuselink into hold der.
c. On test set, set SKI and SVR to positions 1 (fully clockwise); Set SWB, 4,5,6 and 7 to the UP (off) position.
d. Connect vol teeter to test - set terminals, select lob range on a DVM or 25 V range on a conventional meter. Connect power to test set.
f. Insert LDPS card under test into socket with component side of board facing forwards.
4. a.

Set SWB and SW 4 to ON Meter to read 10 to 11 volts. Rotate SKI to position 2. Meter to read 9 to 10 vols.
b.
c. Rotate SKI to position
3. meter to read 13 to 14 volts.
d. Rotate SKI to position 4. Adjust RV1 on LPDS board. so that meter reads 5.10 volts.
5. a.

Set SW to the ON position. Meter will indicate a slight drop (to about 4.9V) in voltage. Leave for 1 minute.
b. After 1 minute touch the body of TR18 and also the surrounding area on the heat si mk. Both should be gently and equally warm
c. Set SWG to the ON position. Meter will indicate a further slight drop in voltage. (to about 4.8 volts)
6. a.

Short circuit the output terminals with a piece of wire or screwdriver. Meter to read about zero (less than $1 / 4$ volt). LED 1 will be out.
b. Set SWG, 5, 4 and 3 to the OFF position. Wit for 5 seconds.

With SUR in position 1 press and rel ease push button, the I amp should go on and then go of $f$.
b. Repeat a further 10 times with SVR in positions 2 thru 11.
c. Rotate SVR to position 12, pressing push button will cause RL1 to operate.
d.
e.
10.
11. a.
b.

## TEST PROCEDURE - MBD BOARD (With Mbt her boar d)

TEST NUMBER

## TEST ROUTI NE

1. a.
b. Cl ean contacts.
c. Mark serial numbers on board with black narker.
2. a. Insert VBD board into appropriate position on notherboard. b. Switch ON - Check "GAMEOVER" I amp is on and that neither the "GONG", "BUZZER" or "I LLUM NATI ON BOARD" I amps are ON, on the notherboard test set.
c. Check that no score is registerd when any of the score pushbuttons are operated.
3. a. Operate "COIN INSERTED" pushbutton once. Check "GAME OVER" I amp goes out and that "BOARD I LLUM NATI ON' I ampoon test set goes ON Check score of "Pl ayer 1" showing 301.
b. Operate COI INSERTED' pushbutton 3 nore times. Check scores of players 2, 3 and 4 show 301 as the pushbutton is repeatedly pressed.

c.
d.
4. a.
b.

Score 285 ( $8 \times 32+16+8+4$ i-1). Check "GAME OVER" I amp comes ON. Check pl ayer I's "WIN" I amp cones ON Check Pl ayer I's score goes to -0-. Check "BOARD ILLUM NATI ON' I amp on test set goes OFF about 1 second after the gane is over. Check that operation of any of the score pushbuttons has no effect.
7. a. Operate "COI N INSERT" pushbutton twice. Operate "Pl ayer Change" pushbutton once to bring player 2 into the game. Score 301 ( $9 \times 32,+8+4+1$ ). Check Player 2's "WN" Iamp goes ON Check pl ayer 2' s score goes to - 0- .
b. Oper ate "COI N INSERT" pushbutton 3 tines, operate "Pl ayer Change" pushbutton to bring Player 3 into the game. Score 301 ( $9 \times 32,+8+4+1$ ). Check player 3's WN I amp goes ON Check Pl ayer 3' s score goes to - 0-.
a.

Switch off power. Renove card and paint col ored stripe across serial number.

## TEST PROCEDURE - SPC BOARD

( Wth Motherboard)

## TEST PROCEDURE

1. $\quad$ a. Check visually for unsol dered $\mathbf{j}$ oints, cold $\mathbf{j}$ oi nts and for sol der spl ashes.
b. dean contacts.
c. Mark serial number on board.
2. a. Insert card into notherboard.
b. Switch on power.
3. Push "Coi $n$ Inserted" button once onl $y$.

4 :
Score 1 - Check Pl ayer I's score reads 300.

| 5. | Score $2-"$ | $"$ | $"$ | $"$ | $"$ | 298. |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 6. | Score 4 | $-"$ | $"$ | $"$ | $"$ | $"$ | 204. |
| 7. | Score 8 | $-"$ | $"$ | $"$ | $"$ | $"$ | 286. |
| 8. | Score $16-"$ | $"$ | $"$ | $"$ | $"$ | 270. |  |
| 9. | Score $32-"$ | $"$ | $"$ | $"$ | $"$ | 238. |  |

10. Press Pl ayer Changeebutton and within the 5 second delay press various scores - check no score regi stered.
11. a. Score sufficient number to "BUST".
b. Check after BUST no further scores are recorded.
12. a. Push "Blayer Change" and score sufficient numbers to win gane. (Game byer lamp will cone on)
b. Check after WN, no further scores are recorded.
13. a. Switch of $f$ power.
b. Renove oard frommotherboard.
c. Strike col ored line across serial number.

## TEST ROUTINE

1. a. Check visually for unsoldered joints, joints that look cold and for solder splashes.
b. Clean contacts.
c. Mark serial number on board with indelible marker.
2. a. Load 4 PSD boards into appropriate places in motherboard..
b. Sitch power on.
c. Press "COIN INSERT" button once - check player 1 display reads 301.
d. Press "COIN INSERT" button 3 more times - check players' 2, 3, and 4 displays read 301.
3. a. Score ${ }_{\| \prime},{ }_{\|}$press "PLAYER CHANGE" once, check player $\frac{1}{3}$ display reads 300 .

| b. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 2 | $"$ | $"$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| c. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 3 | $"$ | $"$ |
| d. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 4 | $"$ | $"$ |

4. a. Score 2, " " " " 1 " 1 "
b. " "
$\begin{array}{lllll}\text { c. } & " & " & " & " \\ \text { d. } & " & " & " & "\end{array}$

$\begin{array}{llll}\text { b. } & " & " & " \\ c . & " & " & " \\ d . & " & " & "\end{array}$
d.

6

| a. | Score 8, | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 1 | $"$ | $"$ | 286 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| b. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 2 | $"$ | $"$ |
| c. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $" 1$ | 3 | $"$ | $"$ |
| d. | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | $"$ | 4 | $"$ | $"$ |

Press "COIN INSERT" button 4 times and check each players display reads 301.
a. a. Score $10(8+2)$ Press "PLAYER CHANGE" once, check Player 1 " " " 291.

| $b$. | $"$ | $"$ | $"$ | $"$ | $"$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $c$. | $"$ | $"$ | $"$ | $"$ | $"$ |
| d. | $"$ | $"$ | $"$ | $"$ | $"$ |



TEST PROCEDURE -- PSD BOARD (With Motherboard)

## TEST NUMBER TEST ROUTINE


12. a. Score $100(32+32+16+16+4)$
51.

| 14 | 11 | 11 | 11 | 11 | 1 | 11 | 11 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 11 | 11 | 11 | 11 | 11 | 2 | 11 | 11 |
| 11 | 11 | 11 | 11 | 11 | 3 | 11 | 11 |
| 11 | 11 | 11 | 4 | 11 | 11 |  |  | 51. 51. 51.

c.
d.

13

| a. | Score | 64 | $(32+32)$ |
| :---: | :---: | :---: | :---: |
| b. | $" 1$ | $"$ | $" 1$ |
| $c$. | $" 1$ | $"$ | $" 1$ |
| d. | $"$ | $"$ | $" 1$ |

* AND THAT BUST LAMP IS ON BEFORE PUSHING PLAYER CHANGE.

14 a. Press "COIN INSERT" button 4 times.


Switch off power. Remove boards. Enter details on appropriate card card index files. Mark with colored marker over serial number.

Remove the type number off all the integrated circuits.

$$
\begin{aligned}
& \text { FD ARD TEST PROCEDURE CrANES } \\
& \text { GR title: - } 3, \neq 5,6 \\
& \varepsilon, 9,10, \cdots \\
& 12,13,14 \\
& \text { The Aflioform Rayber sene } \\
& \text { nhl CHAMME To THAT SHOWN in } \\
& \text { The Trot fincorbute Retort } \\
& \text { The fayer camenae outran is } \\
& \text { COStED }
\end{aligned}
$$

## TEST ROUTI NE

1. $\quad$ a. Check visually for unsol dered $\mathbf{j}$ oints, $\mathbf{j}$ oints that look cold and for sol der spl ashes.
b. $\quad$ ean contacts.
c. Mark serial number on board.
d. Check 100 ohm resistor and 5nF capacitor have been added.
e. Check R3 is 10 K ohns.
2. a. Insert GPM board into appropriate position on notherboard.
b. Switch ON Check 'GAME OVER' I amp is ON
c. Press 'Player Change' pushbutton and check that -it bas no effect.
3. a Press ' Coi $n$ Insert' pushbutton once. Check ' GAME OVER' I amp goes out, Player I's score reads 301, player I's lamp is ON and that no ot her displays are $O N$ on the notherboard (except for the 2 at the l ower right hand side which per manently illum nate the 'Push' for Pl ayer Change' caption.)
b. Press 'Pl ayer Change'. Check it has no effect on the stat us of the notherboard di spl ays.
4. a.
b.
c. Press ' Pl ayer Change' a number of times and check that machine cycles through pl ayers' turns 1-2-1-2- etc as indicated by their respective lamps. (To speed up the testing process a resistor zalue 47K ohns can be placed across R9, for the duration of the renai nder of the testing).
5. a. Press 'Coin Insert' pushbutton once. Check that only player is registered (status as described in 3a).
b. Press 'Coin.Insert' pushbutton twice nore. Check that players 2 and 3 are now registered.
c. Press "Pl ayer Change' a number of times and check that the machi ne cycles thru players' turns 1-2-3-1-2-3 etc.
6. a. Press "Coin Insert" button once. Check that only player is regi stered as bef ore.
b. Press 'Coin Insert' button three nore tines and check all 4 players are now regi stered.
c. Press ' Pl ayer Change' pushbutton a number of times and check the nachi ne cycles thru pl ayers turns 1-2-3-4-1-2-3-4 etc.
7. $\quad$ a. Press ' Pl ayer Change' pushbutton appropriately to activate player 1.
b.
c. Score 16- check player I's score is 285. Repeat 7b for the other 3 pl ayers, checking that each in turn recei ve a score of 285.

TEST PROCEDURE GPM BOARD ( $\mathbf{V} \boldsymbol{*}$ th Mbtherboard)
TEST NUMBER
TEST ROUTI NE
a. a. Press ' Pl ayer Change' sufficient times to activate' player 1.
b. Score $288(9 \times 32)$. The machi ne will indicate a BUST situation. Check that player I's score returns to . 285 .
c. Repeat Bb for the remaining 3 players ensuring that their score returns to 285.
9. a. Score $285(8 \times 32 \mathbf{t} \mathbf{1 6}+8 \mathbf{t 4}+1)$ and check that the ' GAME OVER' I amp is ON
b. Press ' Pl ayer Change' pushbutton and check that it has no effect.

10
a.

Switch OFF power. Renove card and paint a col ored stripe on its serial number. (Renove the temporary 47K ohm resistor if it has been used).

## ASSEMBLY:INSTRUCTIONS FOR HEATSINK ON LDPS CAR:

STAGE 1 - Tbspect heatsink for good clean, burr-free mounting -urfa, e STAGE 2 Lichtly countersink. 12 holes on PC card that coincide with
he tsinkholes, on component side of the card.
STAGE $3-$ Diodes. IN1200 (D4,thru D9)

- Silicongr' e on both sides of mica washer
-Micawashe $\quad$ diode,
-Insul发むing sieeve (maximum length $1 / 8^{\prime \prime}$ ) on diode
- Di ode- through heatsink and p.c. card
- Pl ai n washer
- Locki ng washer
- Nut

> - Do not tighten at this stageRepeat for 5 more di odes

STAGE 4 Transi s 2N3055 (TR18)
a. $\quad$ Si or grease on mica washer and mica washer on transistor
-Sleves on 2 leads (naxi mum length $1 / 8^{\prime \prime}$ )
b. $\quad \mathbf{- 2}$ bolts ( $1 / 2$ or $3 / 4^{\prime \prime}, 6-32$ ) with locking wabber then plain washel

- Through p.c. card and heatsink
- 2 insuldting sleeves (max. I ength $1 / 8^{\prime \prime}$ ) on bolts on heatsin. sid.
c. - Mbunt transistor
- Locking washers and nuts -Do nat tighten - Do not solder-

STAGE 5 Transist or TI P31, 17) and SCR TIC 106P(SCR 1)
a. -Bend l-ads of devices te fit p.c. card hol es
-Silico grease on mica washers and nount mica warbers on devices
b. - 2 jolts (1/2'to $3 / 4^{\prime \prime}, 6-32$ ) with locking washer then pl ain washel

- Through p.c. card and heatsink
-2 sinsulating sl eeves (max. length $1 / 8^{\prime \prime}$ ) on bolts
c. - Monnt devices with 1 eads 1 n p.c.card
- Locking washers and "nuts
- Do not tighten - Do not sol der-

STAGE 6 stighten TR18 bolts

- Ti ghten tiodes'nu's
- Ti ghten TR17 and S bolts

STAGE 7 s Solder Ieads TR1, TR17 and SCR
-Fi appropriate $\begin{aligned} & \text { i } \\ & \text { res } t ~ D 4 ~ t h r u ~ D 9 ~ a s ~ p e r ~ a s s e n b l y ~ d r a w i n g ~\end{aligned}$

```
I NSTRUCTI ON SHEET NO. }3
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## MDTHERBOARD WIRING CHANGES

MACH NES 25 thru 50 $\because$ "PLAYER CHANGE FOR 5 SECS MODN."






SChematic LDPS cAAD DRAWING SAD OI22 SSI 6176


The Gane and Pl ayer Managenent (GPM) card (con't)

IC11 output is used to distribute the score pulse train, PI-09 and this is output as P1-18 a through d to the 4 PSD cards.

The power-on reset circuit is controlled by TR1 and monostable IC21, after about $\frac{1}{2}$ second after turning on power IC21 produces a pulse which as al ready nentioned, sets IC19. Al so a pulse is sent to the WBD card, PO 13 which sets the WN register (this puts the machine in a GAMEOVER condition and so prevents any inputs from having effect intil a coin is put in) and four pulses are dispatched to the PSD cards PO 15 a through d. (On the PSD cards these are used to effect a parallel load of the 3 decade counters. In the case of power up it loads in a score of 301).

The register IC19 previ ously mentioned is buffered and output as L1-31 a through d to the 4 PSD cards. This controls the type of parallel entry of the 3 decade counters, for a new gane it allous 301 to be entered and for a gane in progress itt allows the player last score to be entered.

Fi nally for the GPM card, PI-16 is not used and a spare gate on this card is used by a signal from the VBD card PO. 20 entering and exiting as P1-24.
5.5 The WIN and BUST Detection (VBD) card.
(PL3 on the Mbtherboard)
Inputs LO 12 a through d are from the 4 PSD cards and are the 'borrow signal from the last stage of the score counter. Hence if a player wins, his score stands at zero and LO 12 is at logic 0. However if a player gets nore than is necessary to win, LO 12 will go to zero and return to a logic 1 when the next pulse of the score occurs.

Any LO-12 si gnal triggers monostable IC16. The trail-ing edge of this monostable clocks into 2 registers. The si gnal LO-12 and its inverse. The first register of IC11 is the WIN register (having the inverse of LO 12 cl ocked into it). It outputs LO-15 to the SPC card to prevent any further scoring; LI-14 to the LDPS card and thence to the GAMEOVER Iamp; LI-13 (a result of ANDing with IC6, a 1 second monostable) to the LDPS card and thence to the Board Illumination lanp; and with suitable gating with LI-07 through 10 (which tell whose turn it is anongst the 4 players) it outputs LI-16 through 19 to the LDPS card and thence to the appropriate WIN caption lamps. The WIN register triggers monostable IC14 to produce a pulse to drive the gong.


